IN THE CLAIMS:

Please cancel Claims 47 and 51 without prejudice or disclaimer of the subject matter recited therein.

Claims 1-31. (Cancelled).

32. (Previously Presented) An image display apparatus comprising:

a plurality of display devices wired in a matrix through a plurality of scanning signal wirings and a plurality of modulated signal wirings; and

a driving circuit configured to apply a modulated signal having a modulated pulsewidth to each of said plurality of modulated signal wirings,

wherein said driving circuit has a plurality of transistors connected in parallel to one of the plurality of modulated signal wirings, wherein the plurality of transistors include a first transistor and a second transistor, and a duration of a time period in which the first transistor is in an on state and a duration of a time period in which the second transistor is in an on state are different from each other, and at least a part of the time period in which the first transistor is in the on state and at least a part of the time period in which the second transistor is in the on state overlap.

Claims 33 and 34. (Cancelled).

35. (Previously Presented) The apparatus according to claim 32, wherein at least one of the plurality of transistors is connected to a predetermined potential.

Claims 36-38. (Cancelled).

39. (Previously Presented) The apparatus according to claim 32, further comprising a circuit for determining the operation states of the plurality of transistors.

40. (Previously Presented) The apparatus according to claim 32, wherein said driving circuit comprises a rise circuit for raising the signal level of the modulated signal and a fall circuit for causing the signal level of the modulated signal to fall.

41. (Previously Presented) The apparatus according to claim 32, wherein each said display device comprises an electron-emitting device.

Claims 42-49. (Cancelled).

50. (Previously Presented) An apparatus according to claim 32, wherein the time period in which the first transistor is in the on state partially overlaps the time period in which the second transistor is in the on state.

Claim 51. (Cancelled).